S.NO	**TILTE**
VL 1	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding
VL 2	Design of Power and Area Efficient Approximate Multipliers
VL 3	Content Addressable Memory—Early Predict and Terminate Precharge of Match-Line
VL 4	Overloaded CDMA Crossbar for Network-On-Chip
VL 5	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
VL 6	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA
VL 7	Register-less NULL Convention Logic
VL 8	Multipliers-Driven Perturbation of Coefficients for Low-Power Operation in Reconfigurable FIR Filters
VL 9	Self-Controlled High-Performance Precharge-Free Content-Addressable Memory
VL 10	A 32-nm Subthreshold 7T SRAM Bit Cell With Read Assist
VL 11	Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames
VL 12	A New CDMA Encoding/Decoding Method for on-Chip Communication Network
VL 13	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
VL 14	Design for Testability of Sleep Convention Logic
VL 15	Precharge-Free, Low-Power Content-Addressable Memory

VL 16	A Low-Cost Low-Power Ring Oscillator-Based Truly Random Number Generator for Encryption on Smart Cards
VL 17	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications
VL 18	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels
VL 19	Code Compression for Embedded Systems Using Separated Dictionaries
VL 20	DW-AES: A Domain-wall Nano wire Based AES for High Throughput and Energy-efficient Data Encryption in Non-volatile Memory
VL 21	Variable Latency Speculative Han-Carlson Adder
VL 22	Scan Chain Masking for Diagnosis of Multiple Chain Failures in a Space Compaction Environment
VL 23	Master–Slave Match Line Design for Low-Power Content-Addressable Memory
VL 24	Low-Power Programmable PRPG With Test Compression Capabilities
VL 25	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia
VL 26	Configurable Folded IIR Filter Design
VL 27	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic
VL 28	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications
VL 29	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis

VL 30	Algorithm and Architecture for a Low-Power Content-Addressable Memory Based on Sparse Clustered Networks
VL 31	Asynchronous Domino Logic Pipeline Design Based on Constructed Critical Data Path
VL 32	Low-Power and Area-Efficient Shift Register Using Pulsed Latches
VL 33	Area-Efficient 128- to 2048/1536-Point Pipeline FFT Processor for LTE and Mobile WiMAX Systems